IN THE CLAIMS

Use the following Amended Claims:

1. (Amended) A structure comprising:

a shaped clock signal generator receiving a data signal and generating a Bit Rate Agile (BRA) shaped data information bearing clock signal, said shaped clock signal generator being synchronous or asynchronous with the data bit rate of the received data signal; and

a data signal processor having a receiver port and a control signal generation means for selecting the shaped data information bearing clock signal for further transmission and/or modulation.

2. **Cancel Claim 2 without prejudice.**

3. **Cancel Claim 3 without prejudice.**

4. (Amended) A structure comprising:

a clock processor communicating clock signals to a plurality of data information bearing clock time position shifted and clock shaped signal generators ;

a data interface input encoder providing a clock selector data signal ; and

a switch receiving said clock selector data signal and selecting, based on said clock selector data signal, one of the clock position time-shifted shaped data information bearing clock signals and connecting the selected signal to a data interface output unit;

said data interface output unit coupling the selected signal to a signal transmission medium or to further signal processing.

5. (Amended) A transmit signal processor structure comprising:

a first clock signal generator having a first set of clock shaping data information bearing parameters and generating a first clock shaped signal;

a second clock signal generator having a second set of clock shaping data information

bearing parameters and generating a second clock shaped signal said second set of clock shaping parameters having at least one parameter different from that of the first set of clock signal shaping parameters;

a data input receive circuit selecting one of the said first or second clock shaped signals;

a switch selecting between the first clock shaped signal and the second clock shaped signal ; and

an output interface communicating the selected signal to the transmission medium.

6. (Amended) A spectral efficient data and clock signal processing system comprising:

a data signal and clock signal processor providing a clock modulated data information bearing signal having changeable time positions between the rising edges and falling edges of the modulated data information bearing clock signals;

a digital interface output circuit connecting the clock modulated data information bearing signal to interface with a subsequent signal processor.

7. (Amended) A clock signal modulator comprising:

a data input interface connecting data signals to a clock source; and

a selector switch means which is controlled by the data input interface selecting a data information bearing clock modulated signal having a shorter separation time between the falling edge and rising edge of the clock modulated signal for one state of the data signal and a longer separation time between the falling edge and rising edge of the clock modulated signal for the other state of the data signal.

8. (Amended) A clock converter system comprising:

an input data interface coupled to a clock signal selection means for controlling the selection of an output shaped clock signal ;

clock signal shaping means providing data information bearing clock signals to the clock signal selection means , said clock signal shaping means having one or more different clock signal data information bearing parameters; and

an output signal processor accepting the different clock signal data information

bearing parameter processed clock converted signals.

9. (Amended) A clock modulated signaling system comprising:

an input data interface to provide control signal generation and

selection of shaped data information bearing clock signals;

an interface to provide signal processing to modulate the clock modulated baseband signal using a cross-correlated quadrature modulator system;

an output amplifier receiving the cross-correlated quadrature modulated signal and generating an amplified cross-correlated quadrature modulated signal for transmission to a transmission medium;

a demodulator receiving and demodulating the amplified cross-correlated quadrature modulated signal; and

signal processor means to decode and regenerate the data information bearing clock modulated signal from the received and demodulated signal .

10. **Cancel Claim 10 without prejudice**

11. (Amended) A method comprising steps:

receiving a data signal;

generating a shaped data information bearing clock signal in response to said received data signal;

generating a control signal for selecting said generated shaped data information bearing clock signal;

and processing said selected shaped data information bearing clock signal for transmission or modulation.

12. (Amended) The method in claim 11, wherein said shaped data information bearing clock signal is generated synchronously with a data bit rate of said received data signal.

13. (Amended) The method in claim 11, wherein said shaped data information bearing clock signal is generated asynchronously with a data bit rate of said received data signal.